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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,391	01/23/2004	Melany Ann Richmond	ZIL-555	8983

47713 7590 12/27/2006

IMPERIUM PATENT WORKS
P.O. BOX 587
SUNOL, CA 94586

EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,391	RICHMOND ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received December 4, 2006 for application number 10/764,391 originally filed January 23, 2004. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 and 9-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno et al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno) in view of Lichter et al. (U.S. Patent No. 6,970,045 B1) (hereinafter referred to as Lichter).

As to claim 1, Bongiorno discloses a method comprising: (a) detecting (via 50) whether a first clock signal (from clock source 10) is inadequate (checks to see if clock signal is available), wherein the first clock signal is generated by a first clock circuit (column 4, lines 22-38); (b) decoupling (deselecting via switching means 66 within 60) the first clock circuit (10) from a system clock input lead of a processor, wherein the decoupling is not performed as a result of a signal from the processor (Bongiorno discloses a malfunctioning clock signal being deselected [via switching means 66 within 60] from a processor [80] after watchdog timer [70] sends out a reset signal to the processor; therefore decoupling is performed as a result of the timer [70] and not the processor; Abstract and column 4, line 9 thru column 5, line 12); (c) coupling (selecting) a second clock circuit (20) to the system clock input lead of the processor (Bongiorno discloses a second clock circuit [20] being selected [via switching means 66 within 60] to the processor[80]; Abstract and column 4, line 2 thru column 5, line 12); (e) decoupling (deselecting) the second clock circuit (20) from the system clock input lead of the processor (Bongiorno discloses the malfunctioning clock signal being deselected [via switching means 66 within 60] from a processor [80]; Abstract and column 4, line 61 thru column 5, line 12); and (f) coupling (selecting) a third clock circuit (30) to the system clock input lead of the processor (Bongiorno discloses a third clock circuit [30] being selected [via switching means 66 within 60] to the processor[80]; Abstract and column 4, line 2 thru column 5, line 12).

Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit.

Lichter teaches a redundant clock module wherein the redundant clock (either 24 or 26 within 12) is enabled (powered on) when the first oscillator has failed or is "out of tolerance" (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30). Lichter has the additional feature of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (column 2, lines 11-24).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Lichter at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate as taught by Lichter. One of ordinary skill in the art would be motivated to make this combination of including the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate in view of the teachings of Lichter, as doing so would give the added benefit of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (as taught by Lichter above).

As to claim 2, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the first clock circuit a high-speed, external crystal oscillator, wherein the second clock circuit is a low-speed, internal watchdog timer, and wherein the third clock circuit is a high-speed, internal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock

sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 3, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the detecting is performed by detecting no signal edges of the first clock signal during a time period over which a linear feedback shift register increments to a predetermined value (Bongiorno discloses the timer monitoring the processor clock signal such that a predetermined count value [pre-set time-out period] is incremented, as is known in the art, which can be done with or without an LFSR; column 1, lines 26-39).

As to claim 4, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the second clock circuit generates a signal whose frequency is lower than that of the first clock signal, and wherein the second clock circuit and the processor are parts of a single integrated circuit (column 1, lines 11-25).

As to claim 5, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the coupling the second clock circuit in (c) is not performed as a result of a signal from the processor (Bongiorno discloses a malfunctioning clock signal being deselected from a processor after watchdog timer sends out a reset signal to the processor; therefore decoupling is performed as a result of the timer and not the processor; column 4, lines 9-21 and column 4, line 61 thru column 5, line 7).

As to claim 6, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Lichter further teaches the method wherein the third clock circuit is enabled in (d) by powering up the third clock circuit (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30).

As to claim 7, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method further comprising, between step (a) and step (b): sending an interrupt signal (reset signal) to the processor indicating that the first clock circuit has failed (column 4, lines 9-21).

As to claim 9, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method further comprising, between step (d) and step (e): (g) detecting (via detector 50) whether a second clock signal is inadequate, wherein the second clock signal is generated by the third clock circuit (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

As to claim 10, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the first clock circuit can be coupled to the system clock input lead by a multiplexer, the first clock circuit being coupled to a first data input lead of the multiplexer, wherein the second clock circuit is coupled in (c) to the system clock input lead by the multiplexer, the second clock circuit being coupled to a second data input lead of the multiplexer, wherein a third data input lead of the multiplexer is grounded (inherently grounded as all circuits are grounded), and wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock input lead (column 4, line 61 thru column 4, line 7).

As to claim 11, Bongiorno discloses an integrated circuit, comprising: (a) a processor (80) with a system clock input lead (it is inherent in the art that a processor chip will have a system clock input lead; column 4, lines 2-8); (b) a terminal (element 100 is noted as an "inventive circuit" which necessitates a terminal to receive the clock from circuit 10; column 3, lines 52-57), the terminal coupled to a first clock circuit (10), the first clock circuit generating a first clock signal (column 4, lines 1-8); (c) a second clock circuit (20); (d) a third clock circuit (30); and (e) a clock controller (40) coupled to the system clock input lead (figs. 1A and/or 1B; column 4, lines 2-15), wherein the clock controller is adapted to decouple (deselect via switching means 66 within 60; Bongiorno discloses a failing clock signal [detected by timer 70] being deselected [via switching means 66 within 60] from a processor [80]; column 4, lines 9-34) the system clock input lead from the terminal and to couple (select via switching means 66 within 60; Bongiorno discloses another clock signal being selected [via switching means 66 within 60] to the processor[80] when one delivered has failed [times out as detected by timer 70]; column 4, lines 2-34 and column 4, line 61 thru column 5, line 7) the system clock input lead to the second clock circuit (20) upon detecting that the first clock signal has failed (timed out), and wherein the clock controller is further adapted to select the third clock circuit (30) upon detecting that the first clock signal has failed (Bongiorno discloses a third clock circuit [30] being selected [via switching means 66 within 60] to the processor[80]; column 4, lines 2-34 and column 4, line 61 thru column 5, line 7) (Bongiorno further teaches that "failure" has been detected when timer [70] detects [by a time-out period] a "control failure or a lockup" which, as earlier shown in Bongiorno, comprises a clock failure; column 1, lines 26-39 and column 4, lines 11-17).

Bongiorno fails to explicitly disclose the clock controller is further adapted to turn on the third clock circuit upon detection that the first clock signal has failed.

Lichter teaches a redundant clock module wherein the redundant clock (either 24 or 26 within 12) is enabled (powered on) when the first oscillator has failed or is "out of tolerance" (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30). Lichter has the additional feature of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (column 2, lines 11-24).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Lichter at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate as taught by Lichter. One of ordinary skill in the art would be motivated to make this combination of including the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate in view of the teachings of Lichter, as doing so would give the added benefit of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (as taught by Lichter above).

As to claim 12, Bongiorno in combination with Lichter taught the method in claim 11, as shown above. Bongiorno further teaches the integrated circuit wherein the first clock circuit is a high-speed external crystal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor

(CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 13, Bongiorno in combination with Lichter taught the method in claim 11, as shown above. Bongiorno further teaches the integrated circuit wherein the second clock circuit is a low-speed, internal watchdog timer (column 4, lines 9-15) oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 14, Bongiorno in combination with Lichter taught the method in claim 11, as shown above. Bongiorno further teaches the integrated circuit wherein the clock controller can decouple the system clock input lead from the terminal when the processor is receiving an inadequate first clock signal (column 1, lines 11-25).

As to claim 15, Bongiorno in combination with Lichter taught the method in claim 11, as shown above. Bongiorno further teaches the integrated circuit wherein the clock controller decouples the system clock input lead from the second clock circuit and couples the system clock input lead to the third clock circuit (column 3, lines 8-20).

As to claim 16, Bongiorno in combination with Lichter taught the method in claim 11, as shown above. Bongiorno further teaches the integrated circuit wherein the clock controller comprises a primary clock source fail detect circuit (51), and wherein the primary clock source

fail detect circuit detects whether the first clock signal has failed (is available) (column 5, lines 29-52).

As to claims 17 and 18, they are directed to the integrated circuit of steps set forth in claim 16. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 19, Bongiorno discloses a microcontroller integrated circuit (100) operable with an external first clock circuit (10), the microcontroller integrated circuit (column 1, lines 10-39) comprising: (a) a processor (80) having a system clock input lead (it is inherent in the art that a processor chip will have a system clock input lead; column 4, lines 2-8); (b) a terminal (element 100 is noted as an "inventive circuit" which necessitates a terminal to receive the clock from circuit 10; column 3, lines 52-57) for receiving a first clock signal (via 10) generated by the external first clock circuit (10) (column 4, lines 1-8); (c) a second clock circuit (20); and (d) means for detecting (40; figs. 1A and/or 1B) whether the first clock signal (10) is inadequate (checks to see if clock signal is available; column 4, lines 22-27) and, upon detecting that the first clock signal is inadequate (via timer 70; column 4, lines 8-21), for decoupling (deselecting via switching means 66 within 60) the terminal from the system clock input lead and coupling (selecting via switching means 66 within 60) the second clock circuit (20) to the system clock input lead, wherein the means decouples (deselects) the terminal from the system clock input lead and couples the second clock circuit (20) to the system clock input lead without receiving any signal from the processor (Bongiorno discloses a clock selection circuit wherein a timer [70] that can be a separate circuit from the microprocessor [80] and detects a first clock circuit [10] is inadequate [malfunctioning], deselects the first clock [10] via switching means [66 within 60]

and selects and second clock circuit [20] also using the switching means; column 4, lines 9-34 and column 4, line 61 thru column 5, line 7).

Bongiorno fails to explicitly disclose the clock controller is further adapted to turn on the third clock circuit upon detection that the first clock signal is inadequate.

Lichter teaches a redundant clock module wherein the redundant clock (either 24 or 26 within 12) is enabled (powered on) when the first oscillator has failed or is "out of tolerance" (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30). Lichter has the additional feature of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (column 2, lines 11-24).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Lichter at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate as taught by Lichter. One of ordinary skill in the art would be motivated to make this combination of including the ability to enable (power on) redundant/back-up clock circuits when the primary clock fails or is detected inadequate in view of the teachings of Lichter, as doing so would give the added benefit of detecting "out of tolerance" conditions in addition to failure and seamlessly switching to the redundant clock without shutdown, glitches or system crash (as taught by Lichter above).

As to claim 20, Bongiorno in combination with Lichter taught the microcontroller in claim 19, as shown above. Lichter further teaches the microcontroller wherein the means couples the system clock input lead to ground after decoupling the terminal from the system clock input

lead and before coupling the second clock circuit to the system clock input lead (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30).

As to claim 21, Bongiorno in combination with Lichter taught the microcontroller in claim 19, as shown above. Lichter further teaches the microcontroller wherein the means decouples the second clock circuit from the system clock input lead and couples the third clock circuit to the system clock input lead after the turning on of the third clock circuit (column 2, lines 28-43 and column 19-31 and column 5, lines 48-60 and column 6, lines 17-30).

As to claim 22, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the second clock circuit is a low-power, RC oscillator (column 1, lines 11-25).

As to claim 23, Bongiorno in combination with Lichter taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the third clock circuit is entirely on-chip and does not have an external crystal (column 1, lines 11-25).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno and Lichter as applied to claim 1 above, and further in view of Chen et al. (U.S. Patent No. 6,816,979 B1) (hereinafter referred to as Chen).

Neither Bongiorno nor Lichter teach disabling a detection circuit.

Chen teaches a clock detection circuit wherein the clock detector can be disabled (column 4, lines 38-51). Chen has the additional benefit of detecting and resolving clock speed issues (column 1, lines 26-32).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno, Lichter and Chen at the time the invention was made, to modify the clock switching

circuit of Bongiorno to include the ability to disable clock detector when not needed as taught by Chen. One of ordinary skill in the art would be motivated to make this combination of disabling the clock detector when not needed in view of the teachings of Chen, as doing so would give the added benefit of detecting and resolving clock speed issues (as taught by Chen above).

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Response to Arguments

Applicant's arguments see Applicant Argument/Remarks, filed December 4, 2006, with respect to the rejection(s) of claim(s) 1, 11 and 19 under ***35 USC § 102 and 103*** have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon
10 further consideration, a new ground(s) of rejection is made under ***35 USC § 103*** over Bongiorno et al. (U.S. Patent No. 6,292,045 B1) in view Lichter et al. (U.S. Patent No. 6,970,045 B1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this
15 Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after
20 the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
December 21, 2006